1. PCI Engineering Change Request - Addition of 3.3Vaux signal to Connector

TITLE:	Addition of 3.3Vaux signal to Connector
DATE:	May 21,1997 (Last update: 10/27/97)
AFFECTED DOCUMENT(S):	PCI Local Bus Specification, Revision 2.1, June 1, 1996 PCI Bus Power Management Interface Specification Revision 1.0
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1.1. Clarification / Motivation

The PCI SIG Power Management Working Group has determined that in order to enable PCI bus power management to the full extent that the PCI Bus Power Management Interface Specification, Intel's Instantly Available PC and Microsoft's OnNow initiatives allow, PCI addin devices need a dedicated and guaranteed source of power to keep the wake event card logic active while the rest of the PCI bus is without power. This ECR defines a previously reserved connector pin (14A is proposed) as a 3.3Vaux voltage supply to provide the standard source of power for wake event logic.

Several ***assumptions*** have been made in determining the optimal solution for supplying auxiliary power to PCI Add-In devices:

1. Add-In devices will need to function correctly in existing systems, which do not support Vaux, as well as new Vaux capable systems.
2. The majority of add in devices will not require Vaux
3. Due to item 2 above, systems should not have to provide Vaux capacity to handle worst case loading requirements

The first and third assumptions lead to the need to provide mechanisms for budgeting the total available Vaux power and controlling the power consumption of Vaux capable devices. Power consumption of Vaux capable devices can be handled in one of 2 ways:

1. The motherboard could be designed to control Vaux current to individual slots based on software control
2. The add-in board could be made responsible for regulating it's own current consumption based on software control

The power management working group selected option 2 for this ECR due to assumptions 1 and 2. Add-in boards will need to be able to control their usage of Vaux to operate in legacy systems as well as in Vaux capable systems, and since the majority of cards will not need this capability, there is no need to burden the entire system with the cost. Only cards which wish to consume Vaux power will carry the costs.

PCI SIG Requirements for New Pin

This pin meets the criteria set forth by the PCI SIG for defining a reserved pin.

1) This solves a long term need with broad application

The capabilities enabled by the PCI bus's 3.3Vaux pin address global energy utilization regulations that are becoming increasingly more important to buyers given the shortage of inexpensive, clean energy in many parts of the planet. The governmental energy regulations that will be supportable include, but are not limited to:

- Energy Star USA 30W standby

- White Swan Europe 5W sleeping state
- Blue Angel Europe 5W, "communicating" sleeping state

These new capabilities also enable systems manufacturers to add value to their products by way of improved user experience, and reduced cost of owning/maintaining their computers. In the home, intelligent power management enables a consumer electronics (CE) usage experience. CE user expectations require that the computer, when "off" is capable of returning to a fully operational state very quickly when prompted to do so either by external, or internally programmed "wake" events. When in the "off" state the PC is completely silent (no disks or fans spinning), it consumes less than 5 Watts from the AC plug, and has had its system context saved away enabling quick resumption from the point at which it went to sleep (no more boot process). Wake events could be generated in response to external stimulus (telephone ringing, or push button), or other internally programmed events such as home management and telephony apps. Likewise, in the office, remote LAN manageability over the network in conjunction with power savings is becoming a vital tool for MIS managers to achieve lowered total cost of ownership for their networked PCs. The PC's character transformation is brought about by enabling intelligent power management, and instant availability.

The PCI bus will be well positioned to be at the center of new innovations in these areas by enabling the cheapest and most robust architectural hooks in support of sub 5W, always available (wake capable) PC's.

2) Forward and Backwards compatibility is maintained

Old (legacy) PCI cards will continue to function properly in new systems supporting 3.3Vaux. These PCI add-in cards should not be connecting to any of the reserved pins, and so therefore will not be impacted by voltage on the pin, or have any affect on other PCI-PM compliant cards that are also connected to it. New cards implementing 3.3Vaux will continue to function properly within legacy PCI systems, except that they will not be able to deliver wake events. In order to interoperate within PCI systems that do not implement 3.3Vaux, the PCI-PM compliant add-in card must ensure that under fully powered conditions any, and all logic required for normal operation must draw the necessary current from the PCI bus's Vcc pins[1].

3) The function cannot be reasonably implemented with the existing protocol.

Pursuant to the issues described in the following section, it is the opinion of the Power Management Working Group that a new pin be allocated to the PCI connector. The many issues associated with cost, ease of use, and compatibility have convinced the Working Group that the cleanest architectural solution for fully utilizing the PCI bus's power management capabilities is to deliver the auxiliary power source via a PCI connector pin.

Reasons for a new pin

After lengthy discussions within the working group, and with SIG member respondents via email, we decided to promote the allocation of a dedicated pin for auxiliary power source delivery (3.3Vaux). There were several issues that contributed to this decision. Other less attractive alternatives that were explored are described below:

- ***Proprietary Header/Cable configuration***:

[1] Since in a PCI legacy system 3.3Vaux will not be present at pin 14A.

The header/cable mechanism requires a negotiated connection between the add-in card manufacturer and the motherboard manufacturer. This approach is very unfriendly from an ease of use perspective. Many competing "standards" are already beginning to emerge in the absence of an "inband" auxiliary power pin. Additionally, this solution all but rules out the retail distribution channel for the PCI add-in card manufacturer, who cannot depend on a guaranteed point of compatible connection to the motherboard for the end user. This approach would likely generate support calls.

- ***Rechargeable Battery:***

  An onboard rechargeable battery imposes higher cost, ease of use, and usage experience issues. Supporting a battery for a LAN adapter, for example, where the projected auxiliary power loading is approximately 1 watt, would be costly (in terms of money, and PCB real estate). Assuming that new PCI-PM compliant add-in designs would also target the millions of installed legacy PCI systems, the battery would represent a cost overhead that delivered no value as the legacy systems would not support **PME#** from any state. In addition, circuitry for detecting a low battery would also be required to wake the system each time the battery required a charge. Given the combination of cost, unwieldy physical battery size, and frequent wake events required for charging coupled with long term reliability/disposal issues with NiCad batteries, this solution is believed to be unacceptable.

- ***AC Adapter:***

  The primary issue with this solution is cost. And, as in the case of the battery, it represent a cost overhead with no added value for owners of legacy PCI based systems. Another consideration is additional clutter being introduced around the PC which runs counter to recent efforts at cleaning up the wiring rat's nest surrounding the computer.

- ***Multiplexing the 3.3Vaux supply with an existing Vcc pin on the PCI connector***: Using an existing Vcc pin to multiplex in the auxiliary power source adds complexity, and cost to the motherboard design. This approach requires a per slot solution that must be capable of detecting the presence of:

  ◊ a legacy PCI card
  ◊ a PCI-PM compliant card
  ◊ an empty slot

  Such an approach would deliver the 3.3V auxiliary power source to the multiplexed pin for PCI-PM compliant cards or, by virtue of a short circuit detection scheme[2], determine that a legacy card was plugged into the slot and disconnect the 3.3Vaux source from the pin when the bus was in ***B3***. Without this short detection circuitry a legacy card would attempt to power itself entirely via the single 3.3Vaux/Vcc multiplexed pin when the bus is in ***B3***. Handling the transition period where the main Vcc has been switched off and the presence of a short between the Vcc and muxed pins is detected by seeing the voltage on the muxed pin dropping off introduces significant complexity. For a four slot system the cost of this solution could be as much as $5, or roughly $1.25/slot.

PCI Bus Revision 2.1 Specification Changes

The pages in the PCI Local Bus Specification Revision 2.1 that need to be revised to accommodate this request are as follows:

[2] Detects a short circuit between a standard Vcc pin and the muxed 3.3Vaux/Vcc pin.

Page Number	Change Description
16	Add the following after the **M66EN** pin description: **3.3Vaux** in Optional 3.3 volt auxiliary power source delivers power for use by PCI add-in card logic that will be required in the generation of power management events when the PCI bus Vcc pins have been turned off by software. The use of this pin is specified in the PCI Bus Power Management Interface Specification. A system or add-in card that does not support PCI Bus Power Management must treat the 3.3Vaux pin as reserved.
146	Pin 14A should be changed from **Reserved** to **3.3Vaux** (2 places)
150	Pin 14A should be changed from **Reserved** to **3.3Vaux**(3 places)

Page 139, Section 4.3.2. Reset

Add the following paragraph to the end of the section:

PCI systems that implement support for 3.3Vaux must comply with additional reset requirements. (See the PCI Bus Power Management Interface Specification for details.)

Page 142, Section 4.3.4.2. Sequencing

Add the following paragraph to the end of the section:

PCI systems that implement support for 3.3Vaux must comply with additional voltage sequencing requirements. (See the PCI Bus Power Management Interface Specification for details.)

PCI-PM Specification Changes
(New rev. assumed to be Revision 1.0a)

Add the following term to the Glossary of Terms (1.4.) section:

3.3Vaux; 3.3V auxiliary voltage supply. This auxiliary voltage supply is optionally provided by the PCI system to pin 14A of the PCI expansion connectors. **3.3Vaux** is used to power logic that needs to remain active when the rest of the system is unpowered (e.g. modem ring indicator detection logic). PCI functions that are enabled to draw current from this pin may consume no greater than 375mA. Functions that have not been enabled to draw fully from this pin must draw no greater than 20mA. Only PCI functions that support **PME#** generation from the ***D3$_{cold}$*** state by design may utilize **3.3Vaux** power.

Add the following sections following section 5.4.2. Power Off (D3cold)

5.4.3. 3.3Vaux / *D3$_{cold}$* Card Power Consumption Requirements

When the system is switched from its main supply outputs to the auxiliary power source, strict power budgeting with respect to which slots are allowed to consume full **3.3Vaux** power becomes necessary. PCI functions must draw no more than 20mA through the **3.3Vaux** pin when in ***D3$_{cold}$*** if its **PME_En** bit is cleared.

If a PCI function has been enabled for **PME#** generation (**PME_En** bit is set) prior to having entered into the ***D3$_{cold}$*** state, the PCI add-in card (any single function, or combination of multiple functions) may draw up to 375mA through the **3.3Vaux** pin while in ***D3$_{cold}$***.

5.4.3.1. Auxiliary Power Consumption Reporting

The optional *Data Register* has been defined to enable the reporting of fine granular power utilization data for each of the supported power management states. In order to minimize the cost burden while also ensuring a robust architecture, a three bit field has been defined in the *PMC* register that is required for PCI functions that do not support the *Data Register* yet wish to draw from **3.3Vaux** while in ***D3$_{cold}$***.

PMC(8:6), **("Aux_Current"),** provides a rudimentary power reporting vehicle for PCI functions to indicate their maximum required **3.3Vaux** current. Power budgeting software can then use this data to determine how many PCI functions can be configured for wakeup from ***D3$_{cold}$***. (refer to Table 6 - *Power Management Capabilities* Register)

In Section 3.2.3., Update PMC register description (Table 6) with the required changes (highlighted in red…note that new bit 6 added, and revision number bumped).

PMC - Power Management Capabilities (Offset = 2)

The *Power Management Capabilities* register is a 16 bit read-only register which provides information on the capabilities of the function related to power management. The information in this register is generally static and known at design time.

Table 6. Power Management Capabilities - PMC

Bits	Default Value	Read/ Write	Description
15:11	Device Specific	Read Only	**PME_Support** - This 5-bit field indicates the power states in which the function may assert **PME#**. A value of 0b for any bit indicates that the function is not capable of asserting the **PME#** signal while in that power state. bit(11) XXXX1b - **PME#** can be asserted from ***D0*** bit(12) XXX1Xb - **PME#** can be asserted from ***D1*** bit(13) XX1XXb - **PME#** can be asserted from ***D2*** bit(14) X1XXXb - **PME#** can be asserted from $D3_{hot}$ bit(15) 1XXXXb - **PME#** can be asserted from $D3_{cold}$
10	Device Specific	Read Only	**D2_Support** - If this bit is a "1", this function supports the ***D2*** Power Management State. Functions that do not support ***D2*** must always return a value of "0" for this bit.
09	Device Specific	Read Only	**D1_Support** - If this bit is a "1", this function supports the ***D1*** Power Management State. Functions that do not support ***D1*** must always return a value of "0" for this bit.

08:06	Device Specific	Read Only	**Aux_Current -** This 3 bit field reports the **3.3Vaux** auxiliary current requirements for the PCI function. If the *Data Register* has been implemented by this function: • Reads of this field must return a value of "000b" • *Data Register* takes precedence over this field for **3.3Vaux** current requirement reporting. If **PME#** generation from ***D3cold*** is not supported by the function (*PMC(15)*=0), this field must return a value of "000b" when read. For functions that support **PME#** from ***D3cold***, and do not implement the *Data Register* the following bit assignments apply : **Bit 8 7 6** — **3.3Vaux Max. Current Required** 1 1 1 — 375 mA 1 1 0 — 320 mA 1 0 1 — 270 mA 1 0 0 — 220 mA 0 1 1 — 160 mA 0 1 0 — 100 mA 0 0 1 — 55 mA 0 0 0 — 0 (self powered)
05	Device Specific	Read Only	**DSI** - The Device Specific Initialization bit indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. Note that this bit is not used by some operating systems. Microsoft Windows and Windows NT, for instance, do not use this bit to determine whether to use ***D3***. Instead, they use the driver's capabilities to determine this. A "1" indicates that the function requires a device specific initialization sequence following transition to the ***D0*** uninitialized state. Refer to Section 8.3.
04	0b	Read Only	**Reserved**
03	0b	Read Only	**PME Clock** - When this bit is a "1", it indicates that the function relies on the presence of the PCI clock for **PME#** operation. When this bit is a "0", it indicates that no PCI clock is required for the function to generate **PME#.** Functions that do not support **PME#** generation in any state must return "0" for this field.

02:00	010b	Read Only	**Version** - A value of "010b" indicates that this function complies with Revision 1.0a of the *PCI Bus Power Management Interface Specification*

Add the following sections onto Section 7.2 following all existing text:

PCI systems compliant with the PCI Bus Power Management Interface Specification may also support an optional auxiliary power source (**3.3Vaux**) connecting it to pin 14A of its PCI slot connectors.

3.3Vaux DC Characteristics:

PC system manufacturers who choose to support **3.3Vaux** are required to physically route **3.3Vaux** to all PCI slots on their motherboard. Since most systems support a minimum of four PCI slots, it is essential to account for any auxiliary power required by the PCI slots and to budget the available auxiliary power appropriately.

The following table defines the DC operating environment that a **3.3Vaux** enabled system must deliver.

Parameter	Min	Typ	Max	Units
3.3Vaux	3.0	3.3	3.6	Volts
$I_{MAX\ ENABLED}$	-	-	375 (note 1)	mA
$I_{MAX\ DISABLED}$	-	-	20 (note 2)	mA

Note 1. Upper limit when function is in ***D0***, ***D1***, ***D2***, ***D3$_{hot}$*** or is in ***D3$_{cold}$*** with its **PME_En** bit set.
Note 2. Upper limit when function is in ***D3$_{cold}$*** and its **PME_En** bit is cleared to "0b"

Each **3.3Vaux** enabled PCI add-in card's load on **3.3Vaux** must not exceed 375mA. This requirement applies to the slot, whether the load is represented by a single PCI function or by multiple functions. Like-wise, when a function has entered the ***D3$_{cold}$*** state and its **PME_En** bit has not been set, (enabling it to generate **PME#**), it must then reduce its total slot **3.3Vaux** current consumption to less than or equal to 20mA.

Implementation Note:

Reducing total slot current consumption to less than or equal to 20mA can be accomplished by the add-in card in a number of ways ranging from internally disabling as much logic as possible, to electrically isolating the **3.3Vaux** pin from its auxiliary power plane.

3.3Vaux Minimum Required Current Capacity

At a minimum, systems supporting **3.3Vaux** must be capable of fully powering at least one **3.3Vaux** enabled PCI slot while the PCI bus is in ***B3***. In the case of a 4 PCI slot system for example, the minimum required **3.3Vaux** current capacity for that system would be 435mA (1 enabled slot, and 3 disabled slots).

7.2.1. PCI System Design Requirements

System support for delivery of **3.3Vaux** to the PCI connectors is optional. If however **3.3Vaux** is supported by the system, then all of the following requirements must be met.

7.2.1.1. Power Delivery Requirements

1. **3.3Vaux** must be connected to all motherboard PCI expansion slots.
2. The system must be capable of delivering up to 1.24W (375mA@3.3VDC) to each ***enabled*** PCI expansion slot.
3. The system must be capable of delivering up to 66mW (20mA@3.3VDC) to each ***disabled*** PCI expansion slot.
4. The system's auxiliary power source must be of sufficient capacity to support a minimum of one enabled PCI slot when the bus is in ***B3***.

PCI functions in ***D0***, ***D1***, ***D2***, or $\boldsymbol{D3_{hot}}$ are unconditionally enabled to consume up to the 1.24W limit via **3.3Vaux**. This is consistent with systems that are designed with dual mode power supplies. A dual mode power supply supports two separately tuned (load-wise) power sources for the same voltage reference. In the case of 3.3V, for example, the dual mode power supply will output both a high capacity, high efficiency 3.3V source for heavy "runtime" loads, and a lower capacity, yet reasonably efficient, 3.3V source for lightly loaded "sleeping" states. **3.3Vaux**, when supported by the system, must be connected to PCI connector pin 14A, as the logical "OR" of the two supplies. In this way, under normally powered conditions (the PCI bus is in ***B0***, ***B1*** or ***B2***) all PCI add-in cards, supporting $\boldsymbol{D3_{cold}}$ functionality, connecting to pin 14A may draw up to 375mA from the **3.3Vaux** pin. This voltage multiplexer could be implemented discretely on the motherboard with power switches (FETs) and associated control logic, or it could be integrated into the power supply itself. Regardless of the approach to implementation the voltage must never vary outside of the specified voltage regulation band (see Section 7.2.) when switching between the main source and the lower capacity auxiliary source.

Software controls which slots are enabled for **PME#** generation from $\boldsymbol{D3_{cold}}$ and is responsible for remaining within the system's auxiliary power budget

7.2.1.2. PCI Bus RST# Signaling Requirements

The section entitled "Reset" of the PCI Local Bus Specification requires the assertion of **RST#** whenever the PCI main power rails are out of spec, either when low and ramping on, or low as a result of a power failure event. In systems that do not support **3.3Vaux**, when a power failure event is occurring the assertion of **RST#** causes all PCI devices' output buffers to be floated until such time that power is completely lost. At this point the entire bus is floating, including the **RST#** signal.

With the addition of "programmable power failures", and the **3.3Vaux** power source, two new requirements for **RST#** are added to the existing requirements..

Additional PCI RST# Requirements

- **The central resource of systems that support 3.3Vaux must ensure that the PCI RST# signal remains asserted whenever the PCI bus is in the *B3* state.**

This can be accomplished either by powering the PCI **RST#** output buffer with auxiliary power, or by deploying a weak pulldown resistor on the **RST#** signal (on the motherboard) such that when power is lost at the **RST#** output buffer the signal network will have a low impedance path to ground. With **RST#** asserted whenever the bus is in ***B3***, PCI functions that are in the $D3_{cold}$ state can depend on the low to high transition of **RST#** as a reliable indication that they must internally initialize all volatile portions of their function and transition themselves to the $D0_{uninitialized}$ state.

The following diagram illustrates the required behavior of **RST#** when the bus transitions into, and out of ***B3.*** Refer to the "Reset" section of the PCI Local Bus Specification for existing **RST#** requirements.

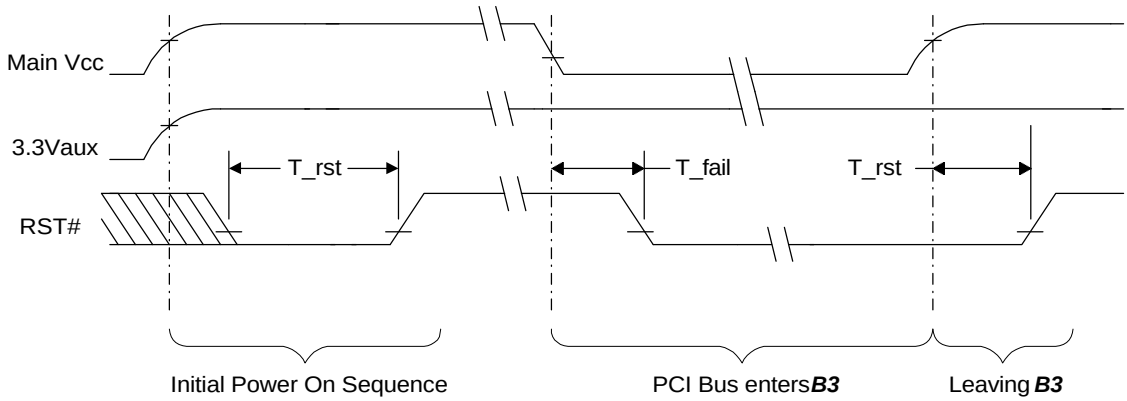

Figure 1. *B3* Reset Timing

- **Functions in $D3_{cold}$ that are capable of generating PME# from $D3_{cold}$ must also be capable of accepting PCI bus cycles, including PCI configuration cycles, no later than 10mS following the low to high transition of the PCI RST# signal**

PCI functions that wake the system with power management events are designed specifically for quick resumption, and must take no longer than 10mS to self initialize to the point where they are ready to accept PCI cycles targeting them.

7.2.1.3. Voltage Sequencing

The **3.3Vaux** power source is independent of the PCI bus's 3.3V and 5V voltage rails, and there are no voltage timing sequencing requirements between them. This is consistent with the sequencing requirements in the PCI Local Bus Specification.

Once all supported voltages have settled to their specified levels **3.3Vaux** must remain within its specified voltage regulation band unless the system has its input AC power source removed. This can occur in one of two ways:

- A mechanical switch is opened, isolating the system from the input AC source.
- An AC power failure (power outage) has occurred

7.2.2. PCI Add-in Card Design Requirements

7.2.2.1. Physical Connection to the 3.3Vaux pin

Only PCI add-in cards implementing functions that support **PME#** from ***D3$_{cold}$*** by design may physically connect to the **3.3Vaux** pin (14A). All other designs must not come into electrical contact with pin 14A, and must only draw current from the main PCI bus voltage rails.

7.2.2.2. Isolation of 3.3Vaux from Main 3.3V

When a PCI add-in card is plugged into a system that supports **3.3Vaux**, the card must ensure that **3.3Vaux** is electrically isolated from the main PCI 3.3V rails at all times. This is done via split power planes with a separate power plane for **3.3Vaux** which never comes into electrical contact with the add-in card's main PCI 3.3V power plane.

In designs where logic paths cross between components powered by the **3.3Vaux** and 3.3V power domains, special care must be taken to ensure that when power is removed from the main 3.3V rail that no physical damage, or logic malfunction occurs with respect to any of the subject devices be they powered or unpowered. The add-in card must electrically isolate these cross-domain powered circuit paths from each other as a direct result of being programmed to the ***D3$_{hot}$*** state. While in ***D3$_{hot}$*** all PCI power rails are still within their specified voltage regulation bands, and the ***D3$_{hot}$*** state is always the initial step towards the eventual removal of main PCI bus power rails. (i.e. ***B3*** / ***D3$_{cold}$***)

7.2.2.3. 3.3Vaux Presence Detection

PCI add-in cards implementing functions that can generate power management events from ***D3$_{cold}$*** must first determine the presence, or absence of 3.3 volts on pin 14A before reporting their support for **PME#** from ***D3$_{cold}$***. A weak pulldown, attached to pin 14A, must be implemented on every PCI add-in card to create a logic low reference when plugged into a motherboard that does not support the delivery of **3.3Vaux**. Note that the current consumed by the pull down resistor must be included in the total slot 3.3Vaux current budget. The function must then logically "AND" this reference with bit 15 of its *PMC* register when read back by the system. In this way functions that normally do support **PME#** from ***D3$_{cold}$*** will report that they do not support it if plugged into a slot without **3.3Vaux**.

Compatibility with PCI Systems that do not support 3.3Vaux

PCI add-in card manufacturers that target both the installed base of PCI systems as well as new PCI systems must ensure that, in a system that does not provide **3.3Vaux** to pin 14A, the card provides a means of powering its split auxiliary power plane using whatever other standard PCI voltage source it has available to it.

The following conceptual diagram illustrates how an add-in card could route power to its auxiliary power plane based upon the presence, or absence of **3.3Vaux** at pin 14A.